This listing of claims will replace all prior versions and listings of claims in the application.

LISTING OF CLAIMS

112. (Currently amended) A semiconductor structure comprising:

a layer structure including a uniform etch-stop layer having a doping level below 10^{18} atoms/cm^3;

~~wherein said uniform etch-stop layer has a relative etch rate which is less than approximately the relative etch rate of Si doped with $7x10^{19}$ boron atoms/cm^3~~.

113. (Previously presented) The semiconductor structure of claim 112, wherein the uniform etch-stop layer is substantially relaxed.

114. (Previously presented) The semiconductor structure of claim 113, wherein the uniform etch-stop layer comprises $Si_{1-y}Ge_y$.

115. (Previously presented) The semiconductor structure of claim 114, wherein $y>0.19$.

116. (Previously presented) The semiconductor structure of claim 113, wherein the uniform etch-stop layer comprises a silicon dioxide layer.

117. (Previously presented) The semiconductor structure of claim 113, wherein a surface of the uniform etch-stop layer is planarized.

118. (Currently amended) The semiconductor structure of claim 112, wherein the layer structure comprises a strained layer disposed over the uniform etch-stop layer.

119. (Previously presented) The semiconductor structure of claim 118, wherein the strained layer comprises $Si_{1-z}Ge_z$ and $0\leq z<1$.

120. (Previously presented) The semiconductor structure of claim 118, further comprising:

an insulator layer disposed over the layer structure.

121. (Previously presented) The semiconductor structure of claim 112, further comprising:
a handle wafer,
wherein the layer structure is bonded to the handle wafer.

122. (Previously presented) The structure of claim 121, wherein the handle wafer comprises an insulator.

123. (Previously presented) The semiconductor structure of claim 121, wherein the handle wafer comprises a material selected from the group consisting of silicon, glass, quartz, and silicon dioxide.

124. (Previously presented) The semiconductor structure of claim 123, wherein the handle wafer comprises a silicon dioxide layer.

125. (Previously presented) The semiconductor structure of claim 112, wherein the layer structure comprises a substantially relaxed layer.

126. (Previously presented) The semiconductor structure of claim 125, wherein the relaxed layer is graded.

127. (Previously presented) The semiconductor structure of claim 126, wherein the relaxed layer comprises $Si_{1-x}Ge_x$.

128. (Previously presented) The semiconductor structure of claim 127, wherein $x<0.2$.

129. (Previously presented) The semiconductor structure of claim 128, wherein the uniform etch-stop layer comprises substantially relaxed $Si_{1-y}Ge_y$ and $y>0.19$.

130. (Previously presented) The semiconductor structure of claim 125, wherein the substantially relaxed layer is disposed over the uniform etch-stop layer.

131. (Previously presented) The semiconductor structure of claim 130, further comprising:
a semiconductor substrate disposed over the relaxed layer.

132. (Previously presented) The semiconductor structure of claim 125, wherein the substantially relaxed layer is disposed under the uniform etch-stop layer.

133. (Previously presented) The semiconductor structure of claim 132, wherein the layer structure comprises a first strained layer disposed over the uniform etch-stop layer.

134. (Previously presented) The semiconductor structure of claim 132, wherein the first strained layer comprises $Si_{1-z}Ge_z$ and $0 \leq z < 1$.

135. (Currently amended) A semiconductor structure, comprising:

a layer structure including a strained Si[[$_{1-z}Ge_z$]] etch-stop layer, and

a handle wafer comprising an insulator, the layer structure being bonded to the handle wafer~~,~~

~~wherein $0 \leq z < 1$~~.

136. (Cancelled)

137. (Currently amended) The semiconductor structure of claim 135, wherein the layer structure includes a ~~substantially relaxed uniform etch-stop~~$Si_{1-y}Ge_y$ layer disposed between[[,]] the strained Si[[$_{1-z}Ge_z$]]etch-stop layer and the handle wafer~~is disposed over the uniform etch-stop layer, $0 \leq z < 1$, and the uniform etch-stop layer has a relative etch rate which is less than approximately the relative etch rate of Si doped with $7x10^{19}$ boron atoms/cm^3~~.

138.–139. (Cancelled)

140. (Currently amended) A[[The]] semiconductor structure ~~of claim 139~~, comprising

a layer structure including a strained $Si_{1-z}Ge_z$ layer, and

a handle wafer comprising an insulator, the layer structure being bonded to the handle wafer,

wherein $0 \leq z < 1$, the layer structure includes a substantially relaxed uniform etch-stop layer disposed over a substantially relaxed layer compris[[es]]ing graded $Si_{1-x}Ge_x$, the strained

$Si_{1-z}Ge_z$ layer is disposed over the uniform etch-stop layer, and the uniform etch-stop layer has a relative etch rate which is less than approximately the relative etch rate of Si doped with $7x10^{19}$ boron atoms/cm^3.

141. (Currently amended) A[[The]] semiconductor structure ~~of claim 139, further~~ comprising

a layer structure including a strained $Si_{1-z}Ge_z$ layer,

a handle wafer comprising an insulator, the layer structure being bonded to the handle wafer; and

an insulator layer disposed over the layer structure,

wherein $0 \leq z < 1$, the layer structure includes a substantially relaxed uniform etch-stop layer disposed over a substantially relaxed layer, the strained $Si_{1-z}Ge_z$ layer is disposed over the uniform etch-stop layer, and the uniform etch-stop layer has a relative etch rate which is less than approximately the relative etch rate of Si doped with $7x10^{19}$ boron atoms/cm^3.

142. (Presently amended) A[[The]] semiconductor structure ~~of claim 139, further~~ comprising

a layer structure including a strained $Si_{1-z}Ge_z$ layer, and

a handle wafer comprising an insulator, the layer structure being bonded to the handle wafer; and

wherein $0 \leq z < 1$, the layer structure comprises a substantially relaxed uniform etch-stop layer and substantially relaxed graded layer disposed over the substantially relaxed layer, the strained $Si_{1-z}Ge_z$ layer is disposed over the uniform etch-stop layer, and the uniform etch-stop layer has a relative etch rate which is less than approximately the relative etch rate of Si doped with $7x10^{19}$ boron atoms/cm^3.

143. (Previously presented) The semiconductor structure of claim 142, wherein the substantially relaxed graded layer comprises $Si_{1-x}Ge_x$.

144. (Currently amended) A semiconductor structure, comprising:

a layer structure including:

a uniform etch-stop layer; and

a strained etch-stop layer disposed over the uniform etch-stop layer, and

an insulator layer disposed over the layer structure~~,~~

~~wherein the uniform etch-stop layer has a relative etch rate which is less than approximately the relative etch rate of Si doped with $7x10^{19}$ boron atoms/cm^3~~.

145. (Currently amended) The semiconductor structure of claim 144, wherein the uniform etch-stop layer comprises substantially relaxed $Si_{1-y}Ge_y$.

146. (Currently amended) The semiconductor structure of claim 144, wherein the strained etch-stop layer comprises $Si_{1-z}Ge_z$ and $0 \leq z < 1$.

147. (Currently amended) A semiconductor structure, comprising:

a[[n]] strained-Si etch-stop layer; and

a substantially relaxed layer disposed over the etch-stop layer.

148.–149. (Cancelled)

150. (Previously presented) The semiconductor structure of claim 147, wherein the substantially relaxed layer comprises $Si_{1-w}Ge_w$.

151. (Previously presented) A semiconductor structure, comprising:

a first uniform etch-stop layer;

a second etch-stop layer disposed over the uniform etch-stop layer; and

a substantially relaxed layer disposed over the second etch-stop layer,

wherein the first uniform etch-stop layer has a relative etch rate which is less than approximately the relative etch rate of Si doped with $7x10^{19}$ boron atoms/cm^3.

152. (Previously presented) The semiconductor structure of claim 151, wherein the first uniform etch-stop layer comprises substantially relaxed $Si_{1-y}Ge_y$.

153. (Previously presented) The semiconductor structure of claim 151, wherein the second etch-stop layer comprises strained $Si_{1-z}Ge_z$.

154. (Previously presented) The structure of claim 153, wherein $0 \leq z < 1$.

155. (Currently amended) A[[The]] semiconductor structure ~~of claim 154~~, comprising:

a first uniform etch-stop layer;

a second etch-stop layer disposed over the uniform etch-stop layer, the second etch-stop layer comprising Si; and

a substantially relaxed layer disposed over the second etch-stop layer,

wherein the first uniform etch-stop layer has a relative etch rate which is less than approximately the relative etch rate of Si doped with $7x10^{19}$ boron atoms/cm^3[[z=0]].

156. (Previously presented) The semiconductor structure of claim 151, wherein the substantially relaxed layer comprises $Si_{1-w}Ge_w$.

157. (Previously presented) The semiconductor structure of claim 151, further comprising:

a handle wafer comprising an insulator,

wherein the substantially relaxed layer is bonded to the handle wafer.

158. (Previously presented) The semiconductor structure of claim 157, wherein the handle wafer comprises a material selected from the group consisting of silicon, glass, quartz, and silicon dioxide.

159. (Currently amended) A[[The]] semiconductor structure ~~of claim 157, further~~ comprising:

a first uniform etch-stop layer;

a second etch-stop layer disposed over the uniform etch-stop layer;

a substantially relaxed layer disposed over the second etch-stop layer;

a substrate disposed over the relaxed layer; and

an insulator layer disposed over the ~~strained~~substantially relaxed layer, between the relaxed layer and the substrate,

wherein the first uniform etch-stop layer has a relative etch rate which is less than approximately the relative etch rate of Si doped with $7x10^{19}$ boron atoms/cm^3.

160. (Currently amended) A[[The]] semiconductor structure ~~of claim 151, further~~ comprising:

a first uniform etch-stop layer;

a second etch-stop layer disposed over the uniform etch-stop layer;

a substantially relaxed layer disposed over the second etch-stop layer; and

a substantially relaxed graded layer,

wherein the first uniform etch-stop layer is disposed over the graded layer and the first uniform etch-stop layer has a relative etch rate which is less than approximately the relative etch rate of Si doped with $7x10^{19}$ boron atoms/cm^3.

161. (Previously presented) The semiconductor structure of claim 160, wherein the substantially relaxed graded layer comprises $Si_{1-x}Ge_x$.

162. (Previously presented) The semiconductor structure of claim 160, further comprising:

a first substrate,

wherein the substantially relaxed graded layer is disposed on the first substrate.

163. (Currently amended) A method for forming a semiconductor structure, the method comprising:

forming a uniform etch-stop layer;

providing a handle wafer; and

bonding the uniform etch-stop layer directly to the handle wafer,

wherein said uniform etch-stop layer has a relative etch rate which is less than approximately the relative etch rate of Si doped with $7x10^{19}$ boron atoms/cm^3.

164. (Previously presented) The method of claim 163, wherein the uniform etch-stop layer comprises substantially relaxed $Si_{1-y}Ge_y$.

165. (Previously presented) The method of claim 163, further comprising:

planarizing a surface of the uniform etch-stop layer prior to bonding.

166. (Currently amended) A[[The]] method ~~of claim 163, further~~ comprising:

forming a uniform etch-stop layer;

providing a handle wafer;

bonding the uniform etch-stop layer to the handle wafer; and

forming a substantially relaxed graded layer before forming the uniform etch-stop layer,

wherein the uniform etch-stop layer is formed over the substantially relaxed graded layer and said uniform etch-stop layer has a relative etch rate which is less than approximately the relative etch rate of Si doped with $7x10^{19}$ boron atoms/cm^3.

167. (Previously presented) The method of claim 166, wherein the relaxed graded layer comprises $Si_{1-x}Ge_x$.

168. (Previously presented) The method of claim 166, further comprising:

releasing the etch-stop layer by removing at least a portion of the graded layer.

169. (Previously presented) The method of claim 166, wherein releasing the etch-stop layer comprises a wet etch.

170. (Previously presented) The method of claim 166, further comprising:

providing a semiconductor substrate,

wherein the substantially relaxed graded layer is formed over the semiconductor substrate.

171. (Currently amended) A method for forming a semiconductor structure, the method comprising:

providing a first substrate; and

forming a layer structure over the first substrate by:

forming a uniform etch-stop layer over the first substrate, the uniform etch-stop layer having a doping level below 10^{18} atoms/cm^3; ~~and~~

~~forming a strained layer over the uniform etch-stop layer,~~

~~wherein the uniform etch-stop layer has a relative etch rate which is less than approximately the relative etch rate of Si doped with $7x10^{19}$ boron atoms/cm^3.~~

172. (Previously presented) The method of claim 171, wherein the etch-stop layer comprises substantially relaxed $Si_{1-y}Ge_y$.

173. (Previously presented) The method of claim 171, wherein the strained layer comprises $Si_{1-z}Ge_z$ and $0 \leq z < 1$.

174. (Previously presented) The method of claim 171, further comprising:
providing a second substrate comprising an insulator; and
bonding the layer structure to the second substrate.

175. (Previously presented) The method of claim 174, wherein the second substrate comprises a material selected from the group consisting of silicon, glass, quartz, and silicon dioxide.

176. (Previously presented) The method of claim 171, further comprising:
forming an insulator layer over the strained layer.

177. (Currently amended) A[[The]] method ~~of claim 171~~, ~~further~~ comprising:
providing a first substrate;
forming a layer structure over the first substrate by:
forming a uniform etch-stop layer over the first substrate; and
forming a strained layer over the uniform etch-stop layer; and
releasing the strained layer by removing at least a portion of the uniform etch-stop layer,
wherein the uniform etch-stop layer has a relative etch rate which is less than approximately the relative etch rate of Si doped with $7x10^{19}$ boron atoms/cm^3.

178. (Previously presented) The method of claim 177, wherein releasing the strained layer comprises a wet etch.

179. (Previously presented) The method of claim 171, wherein forming the layer structure comprises forming a substantially relaxed graded layer and the uniform etch-stop layer is formed over the graded layer.

180. (Previously presented) The method of claim 179, wherein the graded layer comprises $Si_{1-x}Ge_x$.

181. (Currently amended) A[[The]] method ~~of claim 179~~, ~~further~~ comprising:

providing a first substrate;

forming a layer structure over the first substrate by:

forming a substantially relaxed graded layer over the first substrate;

forming a uniform etch-stop layer over the graded layer;

forming a strained layer over the uniform etch-stop layer; and

releasing the strained layer by removing at least a portion of the graded layer and at least a portion of the uniform etch-stop layer,

wherein the uniform etch-stop layer has a relative etch rate which is less than approximately the relative etch rate of Si doped with $7x10^{19}$ boron atoms/cm^3.

182. (Previously presented) The method of claim 181, wherein releasing the strained layer comprises a wet etch.

183. (Currently amended) A method for forming a semiconductor structure, the method comprising:

forming a layer structure by forming a strained $Si[[_{1-z}Ge_z]]$ etch-stop layer, and

bonding the layer structure to a handle wafer comprising an insulator,

wherein $0 \leq z < 1$.

184. (Cancelled) ~~The method of claim 183, wherein z=0.~~

185. (Currently amended) The method of claim 183, wherein forming the layer structure comprises forming a uniform etch-stop layer, the strained $Si_{1-z}Ge_z$ etch-stop layer is formed over

the uniform etch-stop layer, and the uniform etch-stop layer has a relative etch rate which is less than approximately the relative etch rate of Si doped with $7x10^{19}$ boron atoms/cm^3.

186. (Previously presented) The method of claim 185, wherein the uniform etch-stop layer comprises substantially relaxed $Si_{1-y}Ge_y$.

187. (Previously presented) The method of claim 185, further comprising:
forming an insulator layer over the layer structure.

188. (Currently amended) A[[The]] method for forming a semiconductor structure ~~of claim 185, further~~ the method comprising:
forming a layer structure by:
forming a uniform etch-stop layer; and
forming a strained $Si_{1-z}Ge_z$ layer over the uniform etch-stop layer, and
bonding the layer structure to a handle wafer comprising an insulator; and
releasing the strained layer by removing at least a portion of the uniform etch-stop layer,
wherein $0 \leq z < 1$ and the uniform etch-stop layer has a relative etch rate which is less than approximately the relative etch rate of Si doped with $7x10^{19}$ boron atoms/cm^3.

189. (Previously presented) The method of claim 188, wherein releasing the strained layer comprises a wet etch.

190. (Currently amended) A[[The]] method for forming a semiconductor structure ~~of claim 185~~, the method comprising:
forming a layer structure by:
~~wherein forming the layer structure comprises~~ forming a substantially relaxed graded layer; ~~and the~~
forming a uniform etch-stop layer ~~is formed~~ over the substantially graded layer; and
forming a strained $Si_{1-z}Ge_z$ layer over the uniform etch-stop layer, and

bonding the layer structure to a handle wafer comprising an insulator,

wherein $0 \leq z < 1$ and the uniform etch-stop layer has a relative etch rate which is less than approximately the relative etch rate of Si doped with 7×10^{19} boron atoms/cm^3.

191. (Previously presented) The method of claim 190, wherein the relaxed graded layer comprises $Si_{1-x}Ge_x$.

192. (Previously presented) The method of claim 190, further comprising:

releasing the strained layer by removing at least a portion of the graded layer and at least a portion of the uniform etch-stop layer.

193. (Previously presented) The method of claim 192, wherein releasing the strained layer comprises a wet etch.

194. (Previously presented) The method of claim 190, further comprising:

forming an insulator layer over the layer structure.

195. (Previously presented) The method of claim 190, further comprising:

providing a substrate,

wherein the layer structure is formed over the substrate.

196. (Previously presented) The method of claim 195, further comprising:

releasing the strained layer by removing at least a portion of the substrate, at least a portion of the graded layer, and at least a portion of the uniform etch-stop layer.

197. (Previously presented) The method of claim 196, wherein releasing the strained layer comprises a wet etch.

198. (Currently amended) A method for forming a semiconductor structure, the method comprising:

forming a strained etch-stop layer; and

forming a substantially relaxed $Si_{1-w}Ge_w$ layer over the etch-stop layer, wherein $w>0$.

199. (Previously presented) The method of claim 198, wherein the etch-stop layer comprises $Si_{1-z}Ge_z$ and wherein $0\leq z<1$.

200. (Previously presented) The method of claim 199, wherein $z=0$.

201. (Previously presented) A method for forming a semiconductor structure, the method comprising:

forming a first uniform etch-stop layer;

forming a second etch-stop layer over the uniform etch-stop layer; and

forming a substantially relaxed layer over the second etch-stop layer,

wherein the first uniform etch-stop layer has a relative etch rate which is less than approximately the relative etch rate of Si doped with $7x10^{19}$ boron atoms/cm^3.

202. (Previously presented) The method of claim 201, wherein the first etch-stop layer comprises substantially relaxed $Si_{1-y}Ge_y$.

203. (Previously presented) The method of claim 201, wherein the second etch-stop layer comprises strained $Si_{1-z}Ge_z$ and $0\leq z<1$.

204. (Presently presented) The method of claim 203, wherein $z=0$.

205. (Previously presented) The method of claim 201, wherein the substantially relaxed layer comprises $Si_{1-w}Ge_w$.

206. (Previously presented) The method of claim 201, further comprising:

bonding the substantially relaxed layer to a substrate comprising an insulator.

207. (Previously presented) The method of claim 206, wherein the substrate comprises a material selected from the group consisting of silicon, glass, quartz, and silicon dioxide.

208. (Previously presented) The method of claim 206, further comprising:

releasing the second etch-stop layer by removing at least a portion of the first etch-stop layer.

209. (Previously presented) The method of claim 208, wherein releasing the second etch-stop layer comprises a wet etch.

210. (Previously presented) The method of claim 208, further comprising:
releasing the substantially relaxed layer by removing at least a portion of the second etch-stop layer.

211. (Previously presented) The method of claim 208, wherein releasing the substantially relaxed layer comprises a wet etch.

212. (Previously presented) The method of claim 201, further comprising:
forming a substantially relaxed graded layer,
wherein the first uniform etch-stop layer is formed on the graded layer.

213. (Previously presented) The method of claim 212, wherein the substantially relaxed graded layer comprises $Si_{1-x}Ge_x$.

214. (Previously presented) The method of claim 212, further comprising:
bonding the substantially relaxed layer to a substrate comprising an insulator.

215. (Previously presented) The method of claim 212, further comprising:
releasing the first etch-stop layer by removing at least a portion of the relaxed graded layer.

216. (Previously presented) The method of claim 215,
wherein releasing the first etch-stop layer comprises a wet etch.

217. (Previously presented) The method of claim 215, further comprising:

releasing the second etch-stop layer by removing at least a portion of the first etch-stop layer.

218. (Previously presented) The method of claim 215, wherein releasing the second etch-stop layer comprises a wet etch.

219. (Previously presented) The method of claim 217, further comprising:
releasing the relaxed layer by removing at least a portion of the second etch-stop layer.

220. (Previously presented) The method of claim 219, wherein releasing the relaxed layer comprises a wet etch.

221. (Previously presented) The method of claim 201, further comprising:
providing a first substrate; and
forming a layer structure over the first substrate by:
forming a substantially relaxed graded layer over the first substrate;
wherein the first uniform etch-stop layer is formed over the graded layer, and the layer structure comprises the substantially relaxed graded layer, the first uniform etch-stop layer, the second etch-stop layer, and the substantially relaxed layer.

222. (Previously presented) The method of claim 221, wherein the substantially relaxed graded layer comprises $Si_{1-x}Ge_x$.

223. (Previously presented) The method of claim 221, wherein the first uniform etch-stop layer comprises substantially relaxed $Si_{1-y}Ge_y$, the second etch-stop layer comprises strained $Si_{1-z}Ge_z$, $0 \leq z < 1$, and the substantially relaxed layer comprises $Si_{1-w}Ge_w$.

224. (Previously presented) The method of claim 221, further comprising:
bonding the layer structure to a second substrate including an insulator.

225. (Previously presented) The method of claim 224, wherein the second substrate comprises a material selected from the group consisting of silicon, glass, quartz, and silicon dioxide.

226. (Previously presented) The method of claim 221, the method further comprising:

releasing the first etch-stop layer by removing at least a portion of the first substrate and at least a portion of the graded layer; and

releasing the second etch-stop layer by removing at least a portion of the first etch-stop layer.

227. (Previously presented) The method of claim 226, further comprising:

bonding the layer structure to a second substrate prior to releasing the first etch-stop layer.

228. (Previously presented) The method of claim 226, further comprising:

releasing at least a portion of the relaxed layer by removing at least a portion of the second etch-stop layer.

229. (Previously presented) A method for forming a semiconductor structure, the method comprising:

providing a first substrate;

forming a layer structure on the first substrate by:

forming a substantially relaxed graded layer on the first substrate; and

forming a uniform etch-stop layer on the graded layer; and

releasing the etch-stop layer by removing at least a portion of the substrate and at least a portion of the graded layer,

wherein the uniform etch-stop layer of $Si_{1-y}Ge_y$ has a relative etch rate which is less than approximately the relative etch rate of Si doped with $7x10^{19}$ boron atoms/cm^3.

230. (Previously presented) The method of claim 229, wherein the substantially relaxed graded layer comprises $Si_{1-x}Ge_x$.

231. (Previously presented) The method of claim 229, wherein the uniform etch-stop layer comprises substantially relaxed $Si_{1-y}Ge_y$.

232. (Previously presented) The method of claim 229, further comprising:

bonding the layer structure to a second substrate prior to releasing the etch-stop layer.

233. (New) The semiconductor structure of claim 112, wherein said uniform etch-stop layer has a relative etch rate which is less than approximately the relative etch rate of Si doped with $7x10^{19}$ boron atoms/cm^3

234. (New) The semiconductor structure of claim 112, wherein the etch-stop layer comprises n-type dopants.

235. (New) The semiconductor structure of claim 112, wherein the etch-stop layer comprises p-type dopants and the doping level is below 4×10^{16} atoms/cm^3.

236. (New) The semiconductor structure of claim 112, wherein the uniform etch-stop layer is undoped.

237. (New) A method for forming a semiconductor structure, the method comprising the steps of:

forming a MOSFET device having a channel on a substrate,

wherein the channel comprises a portion of a strained Si etch-stop layer.

238. (New) The semiconductor structure of claim 135, wherein the layer structure includes a $Si_{1-y}Ge_y$ layer and the strained Si etch-stop layer is disposed between the $Si_{1-y}Ge_y$ layer and the handle wafer.

239. (New) A method for forming a semiconductor structure, the method comprising:

forming a layer structure including a uniform etch-stop layer;

providing a handle wafer; and

bonding the layer structure directly to a handle wafer,

wherein said uniform etch-stop layer has a relative etch rate which is less than approximately the relative etch rate of Si doped with $7x10^{19}$ boron atoms/cm^3.

240. (New) The method of claim 171, wherein forming the layer structure further comprises: forming a strained layer over the uniform etch-stop layer.

241. (New) The method of claim 171, wherein the uniform etch-stop layer has a relative etch rate which is less than approximately the relative etch rate of Si doped with $7x10^{19}$ boron atoms/cm^3.